REMARKS

This amendment is submitted in response to the Examiner's Action dated October 19, 2006. Applicants have amended the claims to overcome the claim objections. No new matter has been added, and the amendments place the claims in better condition for allowance. Applicants respectfully request entry of the amendments to the claims. The discussion/arguments provided below reference the claims in their amended form.

CLAIMS OBJECTIONS

In the present Office Action, Claims 24 and 32 are objected to. Accordingly, Applicants have amended Claims 24 and 32 to overcome the claim objections. Applicants respectfully request removal of the objections to the claims.

CLAIMS REJECTIONS UNDER 35 U.S.C. § 102

In the present Office Action, Claims 1, 4, 7-9, 21, 23 and 24 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Wang et al.* (U.S. Patent No. 5,187,769). *Wang* does not anticipate Applicants' claimed invention because *Wang* does not teach each feature recited by Applicants' claims. Applicants incorporate herein by reference the arguments proffered in the Amendment dated July 14, 2006.

Applicants' invention provides (1) a vector unit with 2 register files which handles (2) an instruction having two sets of three operands and an opcode which enables parallel processing on the two sets of three operands using an arrangement of (3) multiplexers and (4) two 3-input arithmetic units. Each set of three operands is retrieved (page 4, line 7-9) via multiplexers, from the pair of register files. The two 3-input arithmetic units (ALU 220 and 230) receives an A, B and C input from respective A, B and C multiplexers (*see* page 6, lines 21-31). The arrangement of multiplexers beneficially enables both units to select inputs from either of the two vector register files (page 7, lines 1-2).

The vector unit performs the first operation on a first set of three operands and the second operation on a second set of three operands. Thus, the instruction corresponds to a set of six register operands. Both sets of operands include a first operand, a second operand, and a third

operand, each chosen from respective primary or secondary registers and forwarded to one or both of the arithmetic units.

Applicants' claims recite, in relevant part: (1) "the vector instruction includes a **first** register field indicative of a first primary register in the primary register file and a first secondary register in the secondary register file, a **second** register field ..., **and a third** register field ... in the secondary register file" (Claim 1, *emphases added*); and (2) "the first set of operands includes a **first** operand selected from the first primary register or the first secondary register, a **second** operand ..., **and a third operand** selected from the ... register" (*id.*). Further Claim 4 recites: "the vector unit includes a **3-input primary unit** and a **3-input secondary unit**, wherein the **primary unit** is configured to **perform** the **first operation** on the first set of operands and the 3-input **secondary unit** is configured to **perform** the **second operation** on the second set of operands" (Claim 4, *emphases added*).

Wang is devoid of any teaching of these highlighted features as well as other features of Applicants' claims. That is *Wang* and particularly the cited sections of *Wang* does not teach (or suggest): (a) an instruction having **two** sets of three operands that are placed in (b) two register files which provide, via multiplexers, six inputs into (c) **two** respective **3-input units** (3-input primary and 3-input secondary units).

Rather, in contrast with the above claim features, *Wang* provides a description of a vector coprocessor that includes a set of three parallel **2-input** execution units and a register unit having **three** register files (reference numerals 40, 42, and 44), which respectively feed data into only one corresponding **2-input** execution unit. *Wang*'s system "targets vectors of length 3, and exploits the intrinsic parallelism by providing three parallel execution units that can simultaneously operate on all three vector components." Thus, *Wang* simply discloses three register files which each provide two data inputs to respective ones of three 2-input execution units to execute vector instructions. The referenced sections of *Wang* clearly show the use of register files that provide only **two operands** to **two**-input ALUs.

A set of three data paths feeding from respective three register files into corresponding three 2-input execution units is not synonymous with and does not teach or suggest any of the

above features of Applicants' claims. To restate, *Wang* fails to teach or suggest (a) providing an instruction with two sets of three-operand data, each set including a first, second and third operand, or (b) a 3-input arithmetic unit, or (c) having parallel sets (primary and secondary) of three operand data selected and sent to respective 3-input arithmetic (or floating point) units.

The standard for a § 102 rejection requires that the reference teach each element recited in the claims set forth within the invention. Applicants submit that *Wang* fails to meet this standard and, therefore, Claim 1 (and 4) and all claims dependent thereon are not anticipated by *Wang*. Accordingly, Applicants respectfully requests the Examiner withdraw the § 102 rejection of the above claims.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103

In section 13 of the present Office Action, Claims 22 and 25-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Wang* in view of *Matsuo et al.* (U.S. Patent No. 5,901,301). Further, Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Wang* in view of *Golliver et al.* (U.S. Pub. No. US 2002/0004809). Claims 10 and 22 depend from the above discussed independent Claim 1, which Applicants have shown to be allowable over the primary reference. These claims are therefore allowable over the present combinations, which include the primary reference.

Claims 25 and 31 are further allowable for the same reasons provided above, as these claims clearly recite: (a) "primary and secondary calculating units, wherein the primary **calculating unit includes** first, second, **and third inputs** to receive, respectively, first, second, **and third operands** of a first set of operands and wherein the secondary calculating unit includes first, second, **and third inputs** to receive, respectively, first, second, **and third operands** of a second set of operands; and multiplexing circuitry controlled by the opcode to **select** each of the first, second, **and third operands** ... from the set of primary and secondary file registers..." (Claim 25, *emphasis added*); and (b) "asymmetric instruction includes a set of **three operand register fields** ... wherein the execution unit is configured to perform **a first operation** on a first set of **three operands selected from registers** identified ... and to perform a second operation on a second set of **three operands also selected from the registers**..." (Claim 31, *emphasis added*).

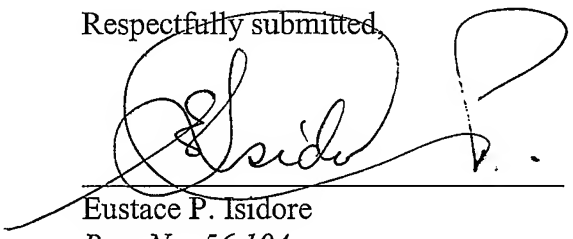
Neither *Wang* nor *Matsuo* teach or suggest, individually or in combination, the above features of Applicants' claims. The limitations with respect to *Wang* have been explained above. *Matsuo* likewise fails to overcome these limitations as *Matsuo* also fails to teach or suggest the pair of three input arithmetic units, which receive three operands from two register files. *Matsuo* merely provides a 3-operand instruction, which is the instruction received by the processing unit. Notably, the 3-operand instruction does not simultaneously provide three operands to a single 3-input arithmetic unit or for that matter to two such arithmetic units. The combination of references thus fail to suggest several important features (previously described above) that are recited by Applicants' claims. As such, one skilled in the art would not find Applicants' invention unpatentable over the combination of references. The above claims are therefore allowable over the combination.

CONCLUSION

Applicants have diligently responded to the Office Action by amending the claims to overcome claim objections. Applicants have also provided discussion/arguments which show why Applicants' claims are not anticipated by or obvious over the references or combinations thereof. Since the arguments overcome the §§ 102 and 103 rejections, Applicants, respectfully request issuance of a Notice of Allowance for all claims now pending.

Applicants further respectfully requests the Examiner contact the undersigned attorney of record at 512.343.6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,



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